# Externally Compensated Op Amps

by Randy Geiger, Updated April 2018

File: Ext Comp OpAmp.docx

 An operational amplifier (Op Amp) is little more than a high-gain amplifier that is designed to be used in a feedback configuration where the feedback gain is ideally independent of the characteristics of the op amp. This independence improves as the gain of an op amp increases but once the gain gets large enough, further improvements in feedback performance with gain are not significant. Op amps can have single-ended or differential inputs and single-ended or differential outputs. By far the most common type of op amp used for discrete applications is the differential-input single-ended output device. In integrated applications, the differential-input, differential-output device is generally preferred though single-ended output devices are useful as well. The op amp can be designed to serve as a voltage amplifier, a current amplifier, a transresistance amplifier, or a transconductance amplifier. Although all types are useful, most op amps designed for discrete applications are viewed as voltage amplifiers. Unless stated to the contrary, emphasis throughout the remainder of this document will focus on differential-input, single-ended output voltage amplifier op amps.

 There are several different architectures that are widely used to build an operational amplifier. Usually these are termed single-stage op amps or two-stage op amps where the number of stages refers to the number of cascaded stages that have a voltage gain. Although cascading more than two stages together to obtain an even larger gain is possible, it is often difficult to maintain stability when feedback is applied. Even the two-stage op amps are vulnerable to problems with stability or ringing/overshoot when feedback is applied. To circumvent these problems, compensation (technically frequency compensation) is applied to the two-stage op amps. The purpose of the compensation is to alter the frequency response of the op amp so that when feedback is applied, the feedback circuit will not only be stable but void of excessive ringing at the output when steps are applied at the input and void of excessive overshoot in the frequency response of the feedback circuit. Invariably the compensation involves moving the open loop poles of the operational amplifier apart far enough so that when feedback is applied they remain well in the left half-plane. Generally the compensation circuit is comprised of a capacitor or of a capacitor and a resistor. A significant effort in the design of many op amps goes into determining how to best provide the compensation.

In the early commercial op amps, a single capacitor was used for compensation and this capacitor was placed external to the op amp. The reason that the compensation capacitor was placed external to the op amp is because the capacitance size required for the compensation capacitor was too large to make it practical to implement the capacitor on-chip. Op amps that use an external compensation capacitor are termed “externally-compensated op amps”. External compensation is rather straightforward and for most op amp architectures, adequate performance of the feedback amplifier can be obtained if the external compensation capacitor is large enough. And, the size of this compensation capacitor can be determined after the op amp is fabricated and after the elements in the feedback network have been selected. Making the capacitor larger than is needed does not compromise the stability of most externally compensated op amps but does limit the closed-loop frequency response so when the feedback circuit is designed to operate at higher frequencies, it becomes important to make the compensation capacitor large enough to eliminate stability, ringing, and overshoot concerns but not so large that it limits the desired frequency response of the feedback amplifier.

Most operational amplifiers that are now available are internally compensated. The compensation network for an internally compensated op amp is internal to the op amp. The introduction of the internally compensated op amp was considered to be a major breakthrough in op amp design since it eliminated the need for the extra pins required for external compensation, the extra cost for the compensation capacitor, and the extra area needed for the external compensation capacitors on printed circuit boards. The uA741 Op Amp released in 1968 was the first internally compensated op amp and it was designed by Dave Fullagar of Fairchild, a 26 year old engineer without much previous experience in op amp design. To make it practical to include compensation capacitors on-chip, it is necessary to make the total capacitance of the compensation network small. Miller compensation is widely used to achieve this goal. With Miller compensation, the signal on one node of a capacitor is an inverted amplified version of the signal on the other terminal. With the Miller compensation, the effective capacitance value is increased by the gain of this amplifier in the Miller compensation network. So, if the gain in the Miller compensation network is -50, this reduces the size of the actual capacitor by approximately a factor of 50 making it practical to put the compensation capacitor internal to the op amp. Since the amplifier in the Miller compensation network is not perfect and since in most internally compensated op amps the second-stage signal path gain amplifier also serves as the Miller compensation amplifier, there is considerable interdependence between the compensation network and the properties of the overall signal-path amplifier. This interdependence complicates the design of the operational amplifier and the design efforts needed to provide the right level of compensation.

The design of an externally compensated amplifier is much simpler. A basic two-stage externally compensated op amp is shown in Fig. 1 Other two-stage architectures could be externally compensated as well.



Fig. 1 Basic two-stage Op Amp

The first and second stages of the op amp have been highlighted on the circuit. The transistors M6, M7, and M8 form a current mirror. A current mirror has an input current and one or more output currents that are proportional to the output current. In the M6:M7:M8 current mirror, the input current is the current IBIAS and the output currents are IT and I2. This current mirror in conjunction with the Bias Current Generator (BCG) generates the bias currents for the op amp. The capacitor CC is the external compensation capacitor. In this circuit, transistors M1 and M2 are sized the same (matched). Likewise, transistors M3 and M4 are matched. Because of the symmetry, the quiescent currents of M1 and M2 are both equal to IT/2.

The design of the op amp primarily involves determining the sizes of M1, M3, and M5 and the bias currents IT and I2. The dc voltage gain of this op amp is given, in terms of the small-signal parameters, by the expression

  (1)

If it is assumed that λn= λp= λ, this can be expressed in terms of the quiescent operating points as

 (2)

where VEB is the excess bias voltage of a transistor,  . In this expression, VGSQ is the quiescent gate to source voltage. For n-channel devices, VEB is positive and for p-channel devices, VEB is negative. The common mode input voltage range is given by

 (3)

This structure has a common-mode input that typically exceeds the supply voltage VDD but the lower range of the common mode input is somewhat larger than VSS.

 The linear output swing is given by the expression

 (4)

## Degrees of Freedom and Design Variables

 Since the gain and signal swings are only a function of the design variable W/L ratios and the bias current IBIAS, this circuit has 7 degrees of freedom; . These degrees of freedom do not appear in the expressions (2),(3), (4) that characterize the operation of the op amp. But the relationship between the design variables and the excess bias voltages that do appear in the design equations can be expressed as

 (5)

We could solve (5) for VEB and substitute back into (2),(3), (4) but the resulting expressions would be quite complicated. It can also be observed that since the gates of M6, M7, and M8 are connected together, VEB6=VEB7=VEB8.

So, we could alternately consider the seven design variables as



From this alternate set of design variables and (5), we can obtain all W/L ratios for devices in the circuit.

 With the square-law device model used in this development, W and L always appear as a W/L ratio. In a more exact model, there is a modest dependence on the values of W and L themselves. Even after the W/L ratio is determined, values for W and L must be determined. In analog circuits, two of the major factors that affect what values should be used for W and L once the ratio is determined are the effects of L on the output conductance and the effects of some other characteristics such as offset voltage on the total channel area. The output conductance, which is ideally zero, degrades for very short devices. As a rule of the thumb, if it is important to have a low output conductance, L should be larger than about 4LMIN where LMIN is the minimum length in a process. In those situations where the area of a transistor, A=WL, is of concern, once the r=W/L ratio is fixed, the length is determined from the expression

  (66)

## Input Offset Voltage

The input-referred offset voltage is of concern in many applications. If good layout strategies are used, this will be dominated by the random offset which is determined primarily by mismatch between M1 and M2 and mismatch between M3 and M4. It can be shown that the standard deviation of the offset voltage of the op amp of Fig. 1 can be expressed as

  (7)

where the parameters AVT0n and AVTop are process parameters that vary somewhat from process to process. In a 0.5µ process, AVTOn and AVT0p are about the same and around 25mV·µ.

This can be alternatively expressed as

  (88)

where A1 and A3 are the channel areas of M1 and M3 respectively. In the latter form, the design variables VEB1 and VEB3 explicitly appear.

 It can be seen that the offset voltage can be reduced by increasing the area of the transistors pairs M1:M2 and M3:M4. For acceptable yield, the area would typically be selected so that

  (99)

## Power Dissipation

The total power dissipation for the amplifier of Fig. 1 is given by the equation

 (9a)

There is considerable flexibility on the relationship between the three currents. A simple solution might be to set IT=I2=5IBIAS.

## *Design Strategy*

 An 8-Step design strategy can now be established by considering  as the independent design variables. From a practical viewpoint, the magnitude of all excess bias voltages should be kept above 100mV. This design strategy follows:

1. Select VEB1 and VEB5 to get the desired voltage gain from (2)
2. Select VEB6 to get the desired output signal swing from (4). (If necessary may need to change VEB5 here and in step 1)
3. Select VEB3 and to get the desired common mode input range from (3). (If the lower end of the input range is not acceptable, may need to adjust VEB6 in Step 2 since VEB6=VEB7).

(if either the common mode input range is unacceptable or the output swing is unacceptable, tradeoffs between gain and signal swing can be made by adjusting VEB1 and VEB3)

1. Select the currents  for acceptable total power dissipation from (9a) (remember )
2. Determine the device ratios (r value) for M1…. M8 from (5)
3. Verify that the W/L ratios are acceptable, if not, tradeoff power for W/L ratios by selecting different bias currents
4. Set the area of M1-M4 to meet offset specifications from (8).
5. Set the lengths of all devices from (6).
6. Set the widths for all devices from the results obtained in step (5) and step (8)
7. Determine CC either through simulations or measurements after fabrication

It is good to avoid minimum length devices because the parameter λ degrades if devices are too short. A rule of the thumb might be to make the minimum gate length at least 4LMIN. This is captured in equation (6). VEB should not be too small either to keep the devices operating in strong inversion. A rule of the thumb might be to limit |VEB |to be greater than 100mV for all devices.

 A simple design that provides good signal swing and reasonably good gain would be simply to make all excess bias voltages equal and set them to 150mV. The currents IT, I2, and IBIAS could all be equal as well.

## Spreadsheet-Aided Design Approach

 From a practical viewpoint, a simple spreadsheet is useful for implementing this design following the 10-step design strategy. The following figure shows such a spreadsheet. Blue shaded cells are where data is entered. Each row in the spreadsheet corresponds to a different design. So the spreadsheet shown is set up for showing 10 designs. The model information that is characteristic of the process is entered in the Model Region. This is fixed for a given process. All design information is entered in the Design Region. The values in the Performance Region and the Device Geometries region are all calculated. The equations behind each of the cells in these latter two regions were given above. The total time required to create such a spreadsheet is likely less than 2 hours. Once a design is completed with the aid of the spreadsheet, a more complete simulation can be run with SPECTRE. Layout can then go directly from the W and L values given in the final implementation in the spreadsheet.

 In this spreadsheet, devices are separated into two groups. Those where the area is critical and those where the area is of little concern. For those where the channel area A is of concern, the channel area is entered and then L and W are calculated from the equations

 (1010)

where r is the W/L ratio obtained from Step 5 in the design flow. For those where channel area is not of concern, L is either LMIN if output conductance is not of concern or 4LMIN if it is important to have a low output conductance. In these cases W is obtained from the equation

  (1111)

In the two-stage op amp of Fig. 1 the area of transistors M1, M2, M3, and M4 are of concern because they affect the offset voltage. The output conductance is of concern if a high dc gain is required.



Fig. 2 Spreadsheet for Design of Externally Compensated Two-Stage Op Amp of Fig.1

When creating the spreadsheet for the op amp of Fig. 1, the W/L values are obtained from (5) which is repeated below as (12). The entries in the (green) L1, L2, L3, L4, W1,W2, W3, and W4 columns are from (13) and (14) for transistors M1, M2, M3, and M4 since the gate (channel) area of these transistors is entered.

 (1212)

 (1313)

 (1414)

The entries for the width (green) columns for the remaining transistors are entered from (11) and the lengths simply copied from the lengths entered in the Design Region (yellow).

## Op Amp Layout

 Layout plays a rather important role in the design of an operational amplifier. The input transistors M1:M2 and the load devices on the first stage, M3:M4 are pair-wise matched. If this matching does not occur, the offset voltage of the op amp can be very large. Because of gradients in threshold voltage, mobility, and oxide thickness across the wafer, a layout that cancels linear gradient effects is essential. Once layout effects are cancelled, area can be increased to reduce the offset voltage as can be seen from (7). The most common method for layout of these transistor pairs is to use what is descriptively termed a common centroid layout. In each pair, the devices are decomposed into either a larger number of parallel devices or, on some cases, parallel and serially connected devices. The layout should be done in such a way that the centroid of the individual segments that comprise one transistor is coincident with that of the matched transistor. The placement of individual segments of two transistors with a common centroid is shown in Fig. 3. In this placement, the blue x is the centroid for the two transistors. The placement of the two segments of one transistor is denoted with the green color and the two segments of the other transistor with the orange color.



Fig.3 A Three Common-Centroid Placements for Two Elements with Two Segments

A more detailed common centroid placement strategy is shown in Fig. 4. In this figure, the purple and green regions are the 24 segments of the two individual transistors. The gold rectangles that surround the common-centroid structure provide isolation from adjacent devices that could also adversely affect the matching performance. The centroid is denoted with the blue **+**.



Fig.4 Placement of Two Devices with 24 Segments Surrounded with Dummy Regions

## Bias Current Generator

The bias current generator could be as simple as a resistor or a diode-connected n-channel or p-channel transistor. With these simple bias current generators, the bias current will be quite sensitive to changes in the supply voltage and will couple noise from the VDD into the op amp. More complicated bias generator circuits are often used that provide a bias current that is nearly independent of VDD. But the topic of bias current generators will not be addressed at this time and for the purpose of obtaining an Op Amp that will work for a project in EE 330, the resistor or diode-connected transistors should work fine.

## Output Stage

The two-stage Op Amp of Fig.1 works well when driving capacitive loads and large valued resistors but does not have good drive capability for driving lower-valued resistive loads. Since the output of the op amp is on the drain terminals of the output devices, M5 and M6, the output impedance is quite large and is given by

  (15)

 A third stage that has lower output impedance can be added to significantly improve the ability to drive resistive loads. Such a stage invariably has a noninverting voltage gain that is near unity so even with an output stage, the amplifier is still termed a two-stage op amp. The most intuitive output stage is simply the common drain amplifier and this is shown in Fig. 5. In this output stage, M10 serves as a bias current generator and is just another output for the M8:M7:M6 current mirror so the gate of M10 is connected to the gate of M8. With the exception of the output signal swing given in (4), the previous expressions for input voltage gain and input signal swing remain the same.



Fig. 5 Common Drain Output Stage

The output swing equation of (4) will be modified if this output stage is used and becomes

 (16)

This is a rather significant reduction in the upper voltage swing. A p-channel common drain amplifier could be used instead and this would limit the lower voltage swing rather than the upper voltage swing and require an additional transistor for generating the bias current. Other output stages that provide larger output signal swings are available.

The spreadsheet of Fig. 2 can be readily modified to include an output stage in the design. In this modification, VEB9 and IOUTQ would be design variables that represent two additional degrees of freedom. The 8-step design strategy can also be readily modified to include provisions for the output stage by adding two steps, one to determine VEB9 and the other to determine IOUTQ. The overall two-stage op amp including the n-channel common-drain output stage is shown in Fig. 6.



Fig.6 Two-stage Externally Compensated Op Amp with Common Drain Output Stage